THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 9

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte MICHAEL D. COOPER

Appeal No. 95-3538
Application 08/108,356[1]

ON BRIEF

Before THOMAS, FLEMING and LEE, Administrative Patent Judges.

LEE, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the final rejection of claims 1-20. No claim has been allowed.

Reference relied on by the Examiner

Ando	5,182,472	Jan. 26, 1993

The Rejection on Appeal

Claims 1-20 stand finally rejected under 35 U.S.C. § 102(e) as being anticipated by Ando.

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[1] Application for patent filed August 18, 1993.

The Invention

The claimed invention is directed to a quasi-complementary BiCMOS circuit having a pull down bipolar transistor and a method for providing a quasi-complementary BiCMOS circuit having a pull down bipolar transistor.

The three independent claims 1, 9 and 17 are reproduced below:

1. A device, comprising:

a quasi-complementary BiCMOS circuit having a pull down bipolar transistor; and

a means for removing shallow saturation charge stored in the pull down transistor's base-collector, said means not utilizing a feedback inverter.

9. A device, comprising:

a quasi-complementary BiCMOS circuit having a pull down bipolar transistor; and

a pull down transistor clamp connected to said pull down transistor, said clamp not utilizing a feedback circuit.

17. A method, comprising:

providing a quasi-complementary BiCMOS circuit having a pull down bipolar transistor; and

providing a means for removing shallow saturation charge stored in the pull down transistor's base-collector, said means not utilizing a feedback inverter.

Opinion

We do not sustain the rejection of claims 1-20 as being anticipated by Ando.

Anticipation is established only when a single prior art reference discloses, either expressly or under the principles of inherency, each and every element of the claimed invention. In re Spada, 911 F.2d 705, 708, 15 USPQ2d 1655, 1657 (Fed. Cir. 1990); RCA Corp. v. Applied Digital Data Sys., Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir. 1984).

Here, all of the appellant's independent claims expressly require a quasi-complementary BiCMOS circuit. Although the term "quasi-complementary BiCMOS" is not defined in the specification, the appellant submits that it is a recognized term in the art and has submitted a trade article in support of the contention. Specifically, during examination and accompanying the response dated August 15, 1994 (Paper No. 4), the appellant submitted a copy of "Quasi-Complementary BICMOS for Sub-3-V Digital Circuits," IEEE Journal of Solid State Circuits, Vol 26, No. 11, Nov. 1991, pages 1708-1719 (hereinafter the "IEEE article").

In the IEEE article from column 1, line 32 to column 2, line 4, quasi-complementary BiCMOS is defined as "[a] BiCMOS circuit that discharges output loads through a composite circuit of pMOS and n-p-n. . . ." In the context of Figure 1(b), the IEEE

article at page 1709 in column 1, lines 4-7, states: "The QC-BiCMOS features the 'quasi-p-n-p' connection, which consists of a pMOS (MP2) and n-p-n bipolar transistor (Q2)." In accordance with Figure 1(b), the pMOS transistor MP2 and the n-p-n bipolar transistor Q2 together form a "quasi p-n-p" component complementary to the n-p-n transistor Q1.

Thus, the appellant has established that the term "quasi-complementary BiCMOS" has a recognized meaning in the art referring to the combination or composite circuit of a pMOS transistor and an n-p-n bipolar transistor. Collectively, it is complementary to an n-p-n bipolar transistor in the circuit. We note further that "BICMOS" has an established meaning in the art referring to circuitry made of both bipolar and CMOS transistors. See U.S. Patent 5,057,713 in column 1, lines 13-14.

The examiner's view that quasi-complementary BiCMOS does not have a recognized meaning in the art is unpersuasive. The examiner points to Iwamura (U.S. Patent 5,057,713) and Young et al. (U.S. Patent 5,111,077) which refer to a circuit employing a pMOS transistor to drive an n-p-n bipolar transistor simply as Bi-CMOS or BiCMOS. But that is not inconsistent with the appellant's position. The term "Bi-CMOS" or "BiCMOS" is broader and covers quasi-complementary type of Bi-CMOS/BiCMOS circuits.

A reading of the examiner's answer reveals that the term "quasi-complementary BICMOS" was not given weight and a BICMOS circuit was deemed sufficient to satisfy the appellant's claims. Throughout the examiner's answer, in discussing the prior art reference Ando, the examiner identified and referred to a BICMOS circuit and not a quasi-complementary BiCMOS circuit.

The appellant is correct in arguing that Ando's Figure 3 embodiment does not disclose or illustrate a quasi-complementary BiCMOS circuit having a pull down bipolar transistor. Specifically, note that the pull down n-p-n transistor Q2 is driven by an nMOS device. We disagree with the appellant's position that Ando's inverter 4 is connected in a feedback arrangement with respect to the output. It is not. However, the lack of a single claim element in a purportedly antipatory reference is sufficient to undermine the rejection as a whole. Here, the missing element is a quasi-complementary circuit which includes a pull down bipolar transistor.

For the foregoing reasons, the rejection of claims 1-20 cannot be sustained.

Conclusion

The rejection of claims 1-20 under 35 U.S.C. § 102(e) as being anticipated by Ando is reversed.

REVERSED

JAMES D. THOMAS Administrative Patent Judge	)
MICHAEL R. FLEMING Administrative Patent Judge	) BOARD OF PATENT) APPEALS AND) INTERFERENCES
JAMESON LEE	)

Administrative Patent Judge)

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